Memory & Logic Based on Spin

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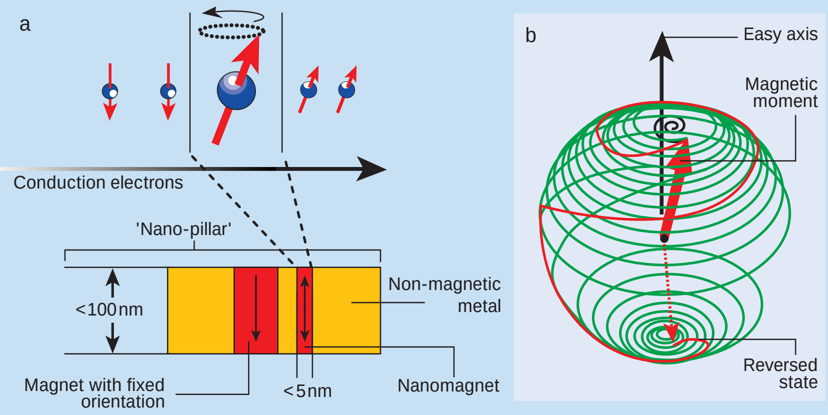
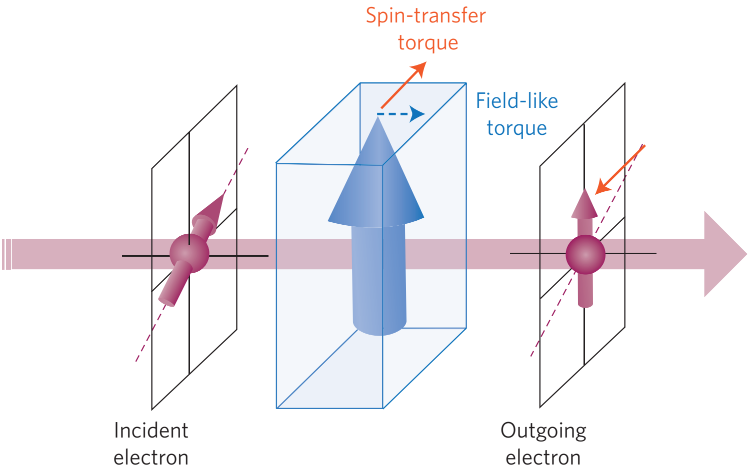
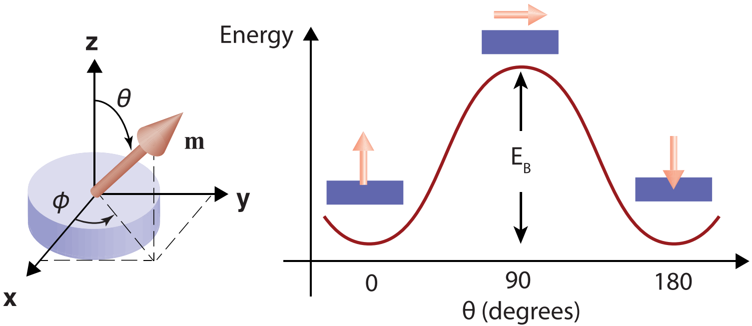
What is Spin?[J.Sun,Nature,2003]



Spin-Transfer Torque Effect



Energy of Spin



Energy & States of Spin

Energy – The energy is the largest at $\theta = 90^{\circ}$

State – The stable state is $\theta = 0^{\circ} or 180^{\circ}$

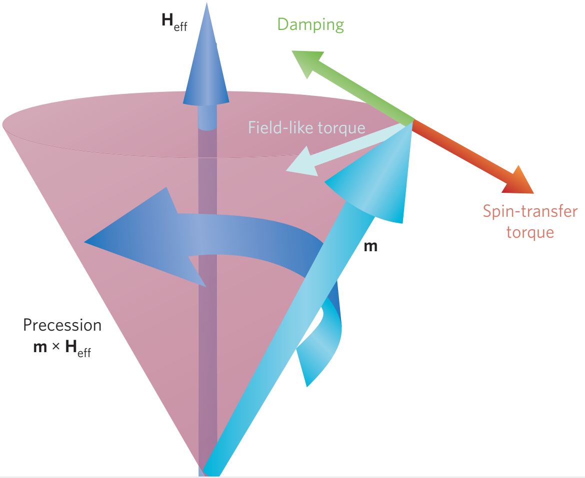
Laudau-Lifshitz-Gilbert(LLG) Equation

LLG equation models the behavior of the magnetization, m, of a nano-magnet in the presence of an effective magnetic field, H_{eff}, and a spin current, Is[A. Brataas,nature,2012].

$$\frac{\partial \mathrm{m}}{\partial t} = \underbrace{-|\gamma| (\mathrm{m} \times \mathrm{H}_{eff})}_{\text{Precession}} + \underbrace{\alpha \left(\mathrm{m} \times \frac{\partial \mathrm{m}}{\partial t} \right)}_{\text{Damping}} - \underbrace{\frac{1}{qN_s} \mathrm{m} \times (\mathrm{m} \times \mathrm{I}_s)}_{\text{Spin torque}}$$

Where N_s is the number of spins comprising the nano-magnet given as $N_s = \frac{M_s V}{\mu_B}$, M_s is saturation magnetizationand, V is the volume of the nano-magnet, μ_B is the Bohr magneton.

Details in LLG Equation



Current-Induced Domain Wall Motion

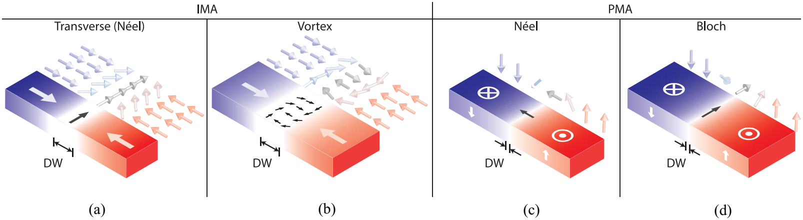
There are 4 kinds of DMs.

Direction of Magnetic Anisotropy

IMA – In-plane magnetic anisotropy
PMA – Perpendicular magnetic anisotropy

- Néel wall occurs in thin and narrow nanostrips
- Vortex or Bloch wall occurs when the nanostrip is wider and thicker

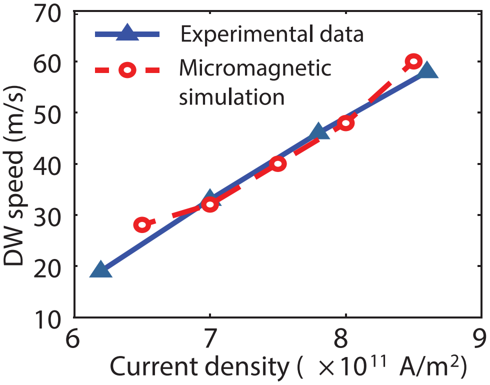
Current-Induced Domain Wall Motion



- (a)&(c) accurs in thin and narrow nanotrips[R.D,IEEE,1997]
- (b)&(d) accurs in wider and thicker nanotrips [Y.Nakatani,Magn,2005]

Electrical current through the DWS could drive a DW in the direction of electron flow.[L.Berger,APL,1978]

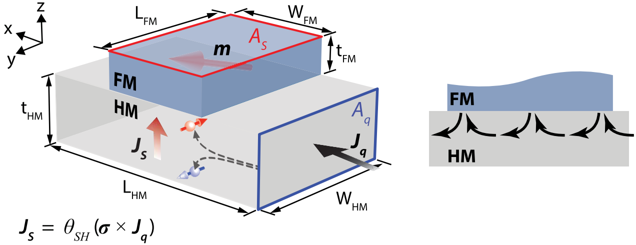
Current-Induced Domain Wall Motion



Simulation parameters

param.	values
α	0.02
K_U	3.5×10^5 J/m^3
M_S	6.8×10^5 A/m
A_{EX}	1.1×10^{-11} J/m
P	0.6

Spin-Orbit Torques(SOT)



(a) (b)

- Spin current: $I_s = \theta_{SH}\frac{A_s}{A_q}I_q\sigma$
- I_s can be larger than I_q for scattering

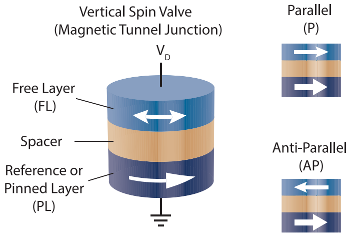
Topological Insulators

Properties

Behavior – Like a quantum Hall insulator
Current – Similar to SOT

- More efficient than SOT.
- Can improve energy efficiency of spin devices for ultralow power computing at room temperature.
- Haven't found any references designing based on this.

Vertical Spin Valve



Tunneling magneto-resistance(TMR)[S.Ikeda,IEEE,2007]

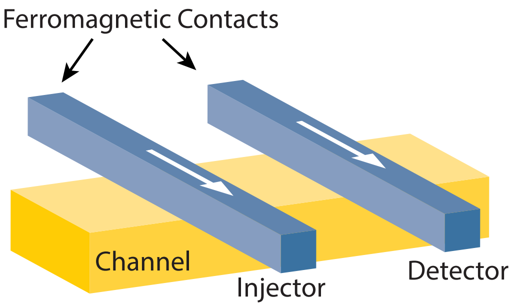
Layer – Pinned layer & Free layer

Spacer – Insulator

Function – Conductance is high(P) or low(AP)

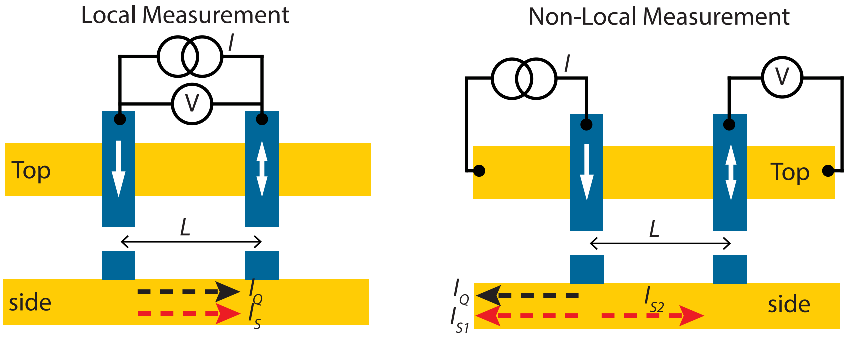
Resistance – $R = \left(\frac{R_P + P_{AP}}{2} + \frac{R_P - R_{AP}}{2}\right) cos\theta$

Lateral Spin Valves



- Both injector and detector are FM
- The channel is NM
- Local & nonlocal measurements

Lateral Spin Valves



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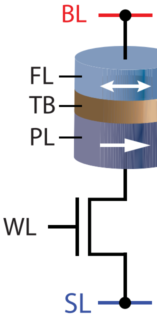
Basic Structure



1T-1MTJ Bit-cell

Write Operation

- WL is charged to V_{DD}
- **'0'** $BL \rightarrow V_{DD}$; $SL \rightarrow V_{SS}$
- **'1'** $BL \rightarrow V_{SS}$; $SL \rightarrow V_{DD}$
- V_{DD} in '0' is smaller than that in '1'

Read Operation

- WL is charged to V_{DD}
- Give a current then compare voltage and vice versa.

Benefits & Issues

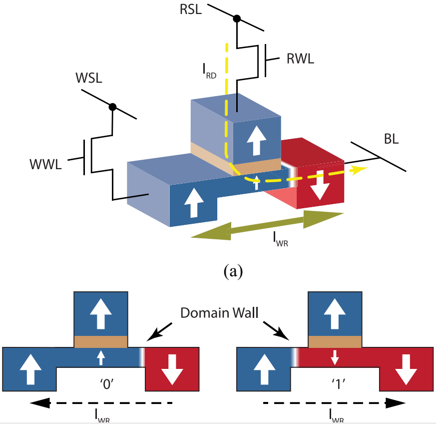
Benefits

1) Nonvolatile can be powered off
2) Itegration density can be $3-4\times$ than that of SRAMs
3) The half-select issue in SRAM is absent due to nonvolatile
4) STT-MRAM arrays may be embedded with new functionality at almost no cost.

Issues

1) High write energy
2) Read/write stability
3) Oxide reliability

Domain Wall Based MTJ Structure



Writing Operation

- $WWL \rightarrow V_{DD}$
- **'0'** $BL \rightarrow V_{DD}$; $WSL \rightarrow V_{SS}$
- **'1'** $BL \rightarrow V_{SS}$; $WSL \rightarrow V_{DD}$

Reading Operation

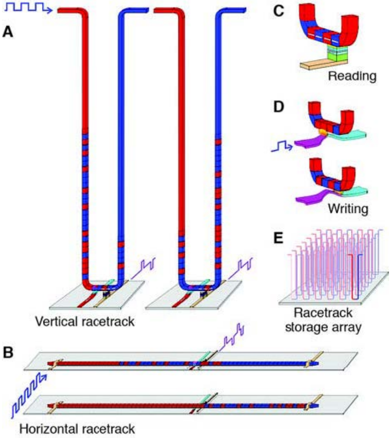
- $RWL \rightarrow V_{DD}$
- Same as the basic device discussed before.

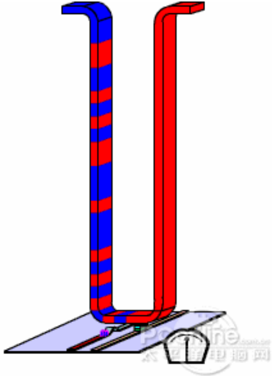
Improvement

Benefits

- Separation of read and write rurrent path.
- Low resistane in the write current path.
- Large write current doesn't flow through tunnel oxide, the reliability is improved.
- Distinguishability between states in the DWMTJ can be improved by using a thicker tunneling oxide, leading to better cell TMR ratio.

Racetrack Memory[IBM,Science,2008]





Racetrack Memory

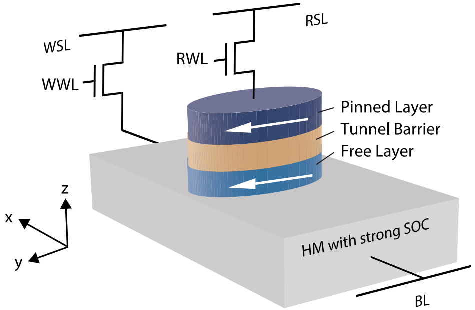
Benefits

- Extremely high integration density.
- Average access time will be $10 - 50ns$ while HDD and MRAM are $(5ms)$ and $(> 10ns)$ perspectively.

Issues

- High current density.
- Thermal noises.
- The latency can cause the access time to be large and variable.

Spin-Orbit Torque Based MTJ Memory Device



Writing Operation

- $WWL \rightarrow V_{DD}$
- **'0'** $BL \rightarrow V_{DD}$; $WSL \rightarrow V_{SS}$
- **'1'** $BL \rightarrow V_{SS}$; $WSL \rightarrow V_{DD}$

Reading Operation

- $RWL \rightarrow V_{DD}$
- Same as the basic device discussed before.

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Characteristics for logic

Five essential points:[Behtash, Nature.nano, 2010]

- Concatenability Input and output should be in the same form.
- Nonlinearity The input and output should be bistability ,i.e. one should provide digitization of information.
- Nonreciprocal Output shouldn't influence the input.
- Gained Output must be charged by indenpendent sources.
- Constructable All other logic functions can be constructed based on a minimal set of operations.

Normally-off Computing

Instant-on & Normally-off Computing[K.Ando,APL,2014]

- The present computers are designed on the premise that power will always be supllied.
- Normally-off computer is only suplied while operating.

Requirement of Normally-off computer

- Non-volatile devices that don't require a power supply to remain inforemation.
- High speed operation to manipulate the information.

Normally-off Computing

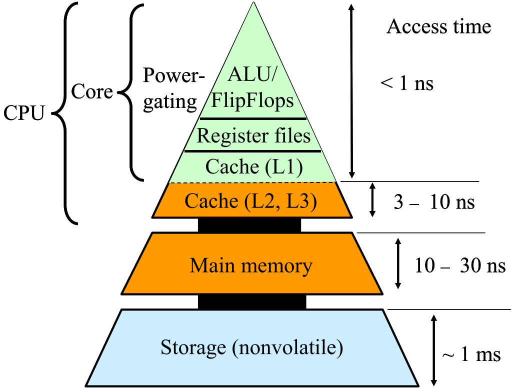


Figure: Layered structure of computer systems.

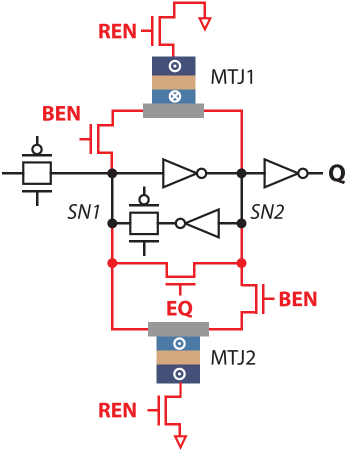
Advantages

- High density
- High speed

Advantages

- MRAM technologies have made marvelous advances
- Effective power reducts by over 80% in mobile CPU [H.Yoda,IEEE,2012]

Normally-off Computing[K.W.Kwon,IEEE,2014]



Backup Operation

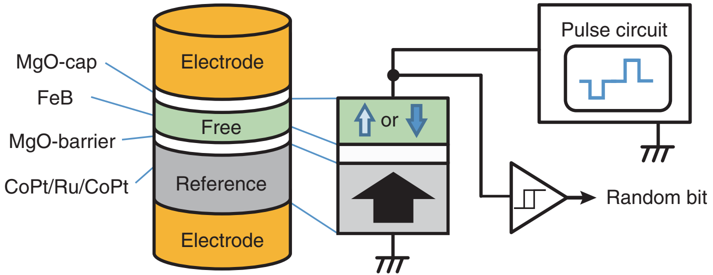
Turn on BEN.

Resume Operation

EQ=1, REN=0
EQ=0, REN=1.

True Random Number Generators[Akio,APL,2014]

- PRNGs are implemented in software and use deterministic algorithms to generate a sequence of RNs.
- For highly secure data encryption we need TRNGs, which are implemented in hardware.



True Random Number Generators

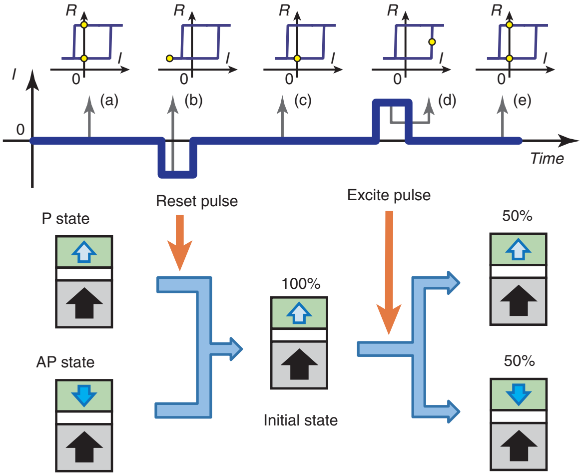
1) Reset to a known magnetization state;
2) Switch with probability of 0.5;
3) Read the generated random bit. Compared.

Switching Probability

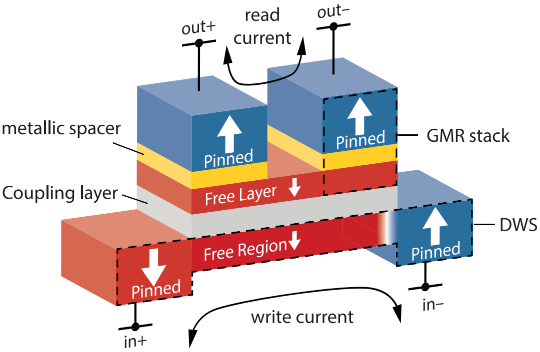
$$P_{SW} = 1 - exp\left\{-\frac{t}{\tau_0} exp\left[-\Delta\left(1 - \frac{I}{I_{c0}}\right)\right]\right\}$$

Where t is the duration of the current pulse, τ_0 is the attempt time, Δ is the thermal stability parameter of the nanomagnet, and I_{c0} is the critical switching current at $0K$.

True Random Number Generators



All-Metallic Logic



- Coupling layer can be *p* or *n* type.
- Similar to *pMOS* and *nMOS*.

All-Metallic Logic[Daniel, DAC, 2012]

Advantages & Disadvantages

Lower voltage supplied – Sub-100mV.
Higher leakage and worsen energy efficiency.

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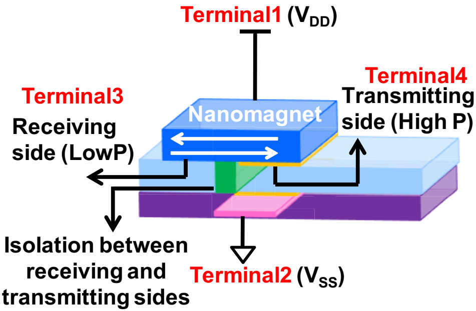
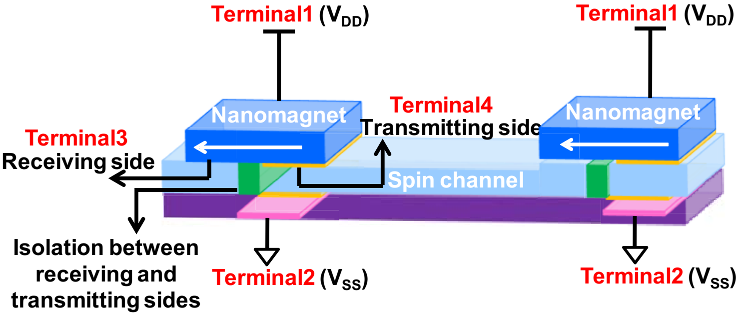
A general ASL devices[C.Augustine,IEEE,2011]

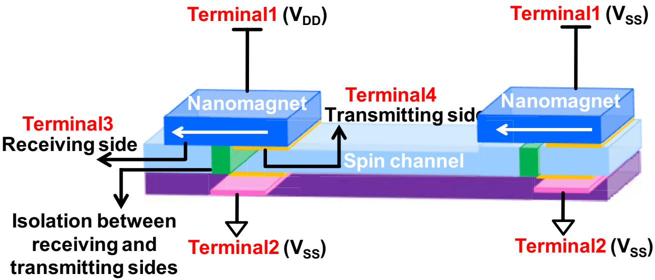


- **Concatenability**
  Spin orientation.
- **Nonlinearity**
  Energy and angle.
- **Nonreciprocal**
  T_3 & T_4.
- **Gain**
  Independent VDD.
- **Constructable**
  Will discuss later.

ASL with no Clock

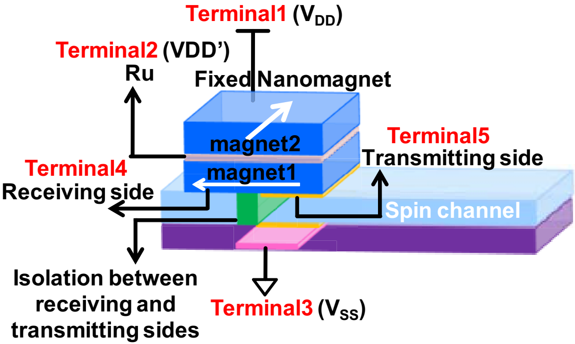


ASL with Clock



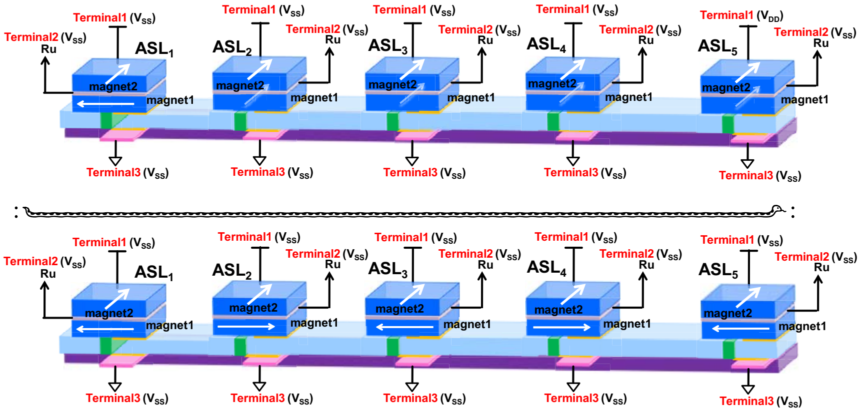
- Not rely on standby power. VDD is supplied only when information propagation.
- Not have to rely on the difference in polarization (highP and lowP) of input and output terminals.

ASL with Clock with Biaxial anisotropy



+ Switching time of ASL_CB can be less than 5*psec* while the former two devices are more than 50*psec*.

ASL with Clock with Biaxial anisotropy



Majority gate[Sheldon, SSCTLD, 1962]

Definition Majority gate

For a majority gate function M, we have the following result, where N_1 and N_0 are number of 1 and 0.

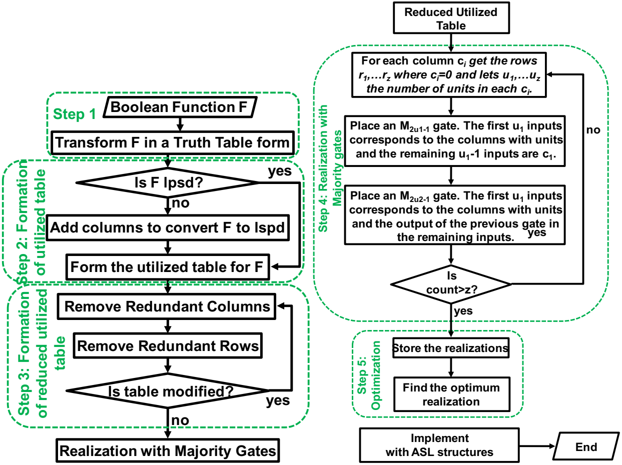
$$M(x_1, x_2, \ldots, x_k) = \begin{cases} 1, & N_1 > N_0 \\ 0, & N_1 < N_0 \end{cases}$$

Theorem

A switching function F can be realized with only majority gates iff for any two n-bit input combinations, r_i and r_j, there exists an x_k such that

$$r_{ik} = F(r_j) \quad and \quad r_{jk} = F(r_j)$$

Implementation of Majority gate

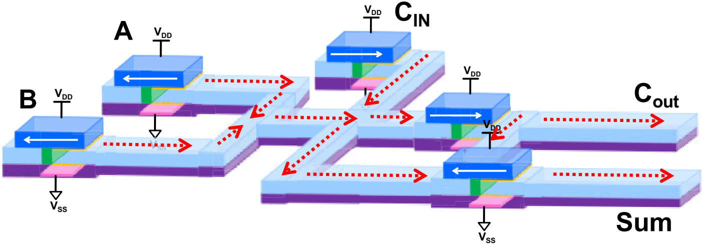


Functionality Enhanced ASL

An example of FEASL – All Adder Implementation.

$$C_{out} = M_3(A, B, C_{in})$$

$$Sum = M_5(A, B, C_{in}, \bar{C}_{out}, \bar{C}_{out})$$



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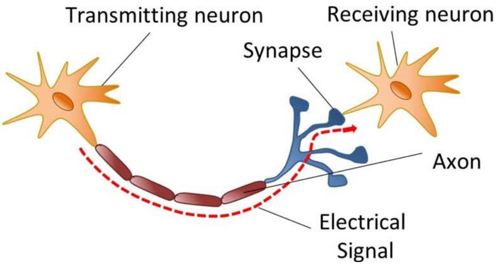
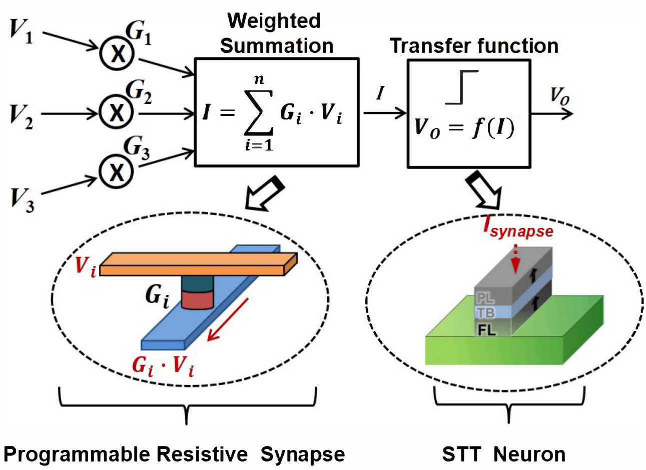
Neuromorphic Computing

Why we use Neuromorphic Computing?

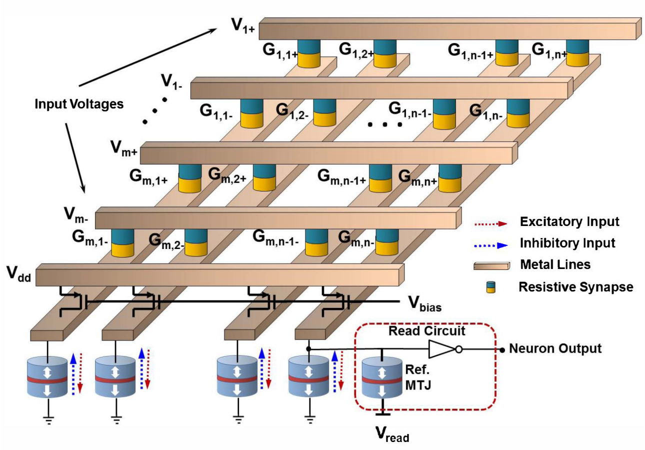
- Extremely efficient in perception and cognition
- Significantly less power and area



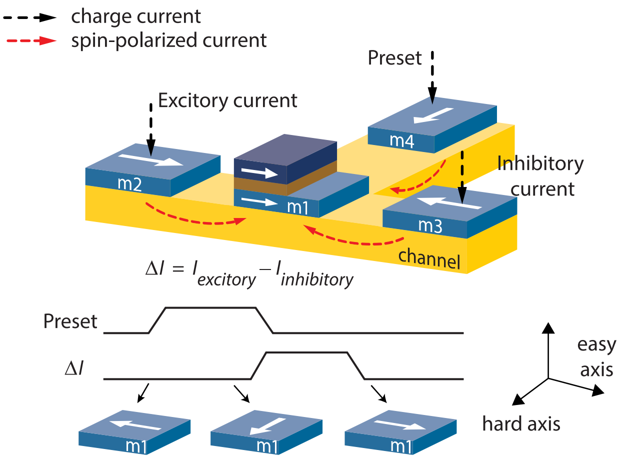
STT Magnetic Neuron[A.Sengupta,IEEE,2015]



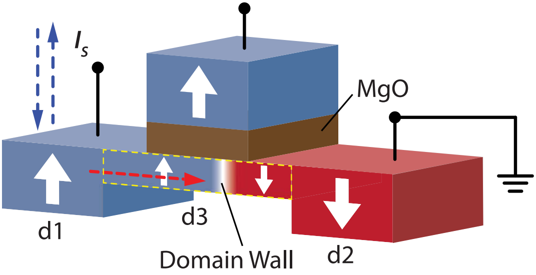
STT Magnetic Neuron



Bipolar Lateral Spin Valve Neuron

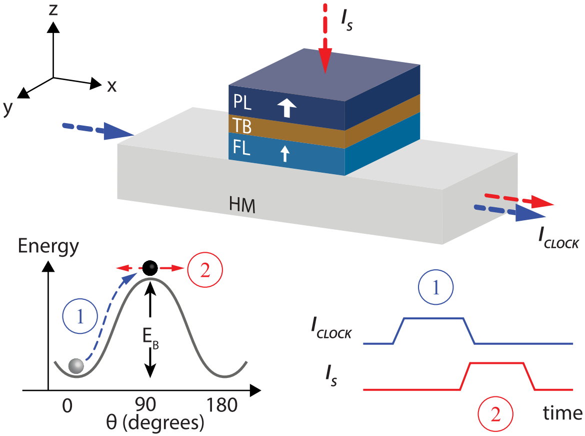


Unipolar Domain Wall Neuron



- Direction of I_S presents excitory or inhibitory.

Unipolar Spin Hall Effect Neuron



Soft-Limiting Nonlinear Neuron

SNN are preferrd in challenging pattern recognition.

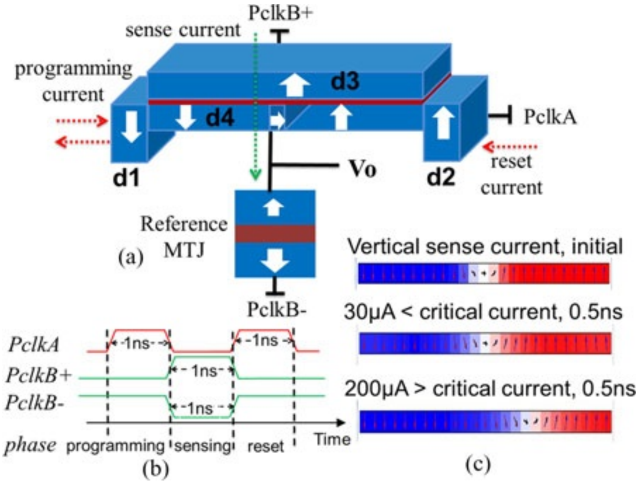
Definition

SNN is neuron with intermediate outputs between the two extreme states.

Improved modeling capacity

- Higher network accuracy
- Lower network complexity

Soft-Limiting Nonlinear Neuron[D.Fan,IEEE.nano,2015]



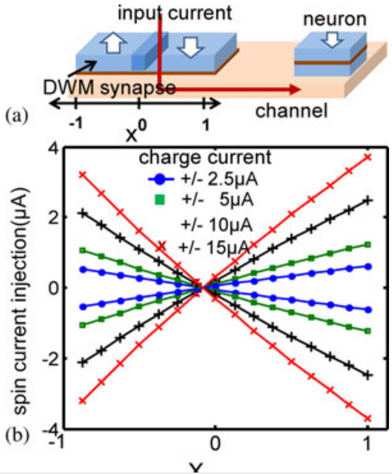
Soft-Limiting Nonlinear Neuron[D.Fan,IEEE.nano,2015]

$$R_{neuron} = \frac{A}{Bx + C}$$

Where A, B, C are constants.

$$\begin{aligned} V_0 &= V_s \frac{R_{ref}}{R_{ref} + R_{neuron}} \\ &= V_s \left(1 - \frac{A}{R_{ref} Bx + R_{ref} C + A}\right) \end{aligned}$$

DW Synapse[M.Sharad,IEEE.trans.nano,2012]



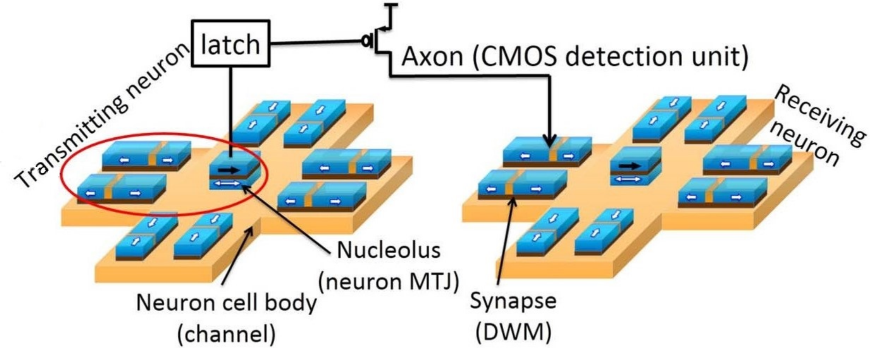
Binary Weights

- Location of DW
- Length of channel

Benefits & Issues

- Logic synthesis and pattern recognition
- Require larger number of neurons for a given operation

DW Synapse Based ANN



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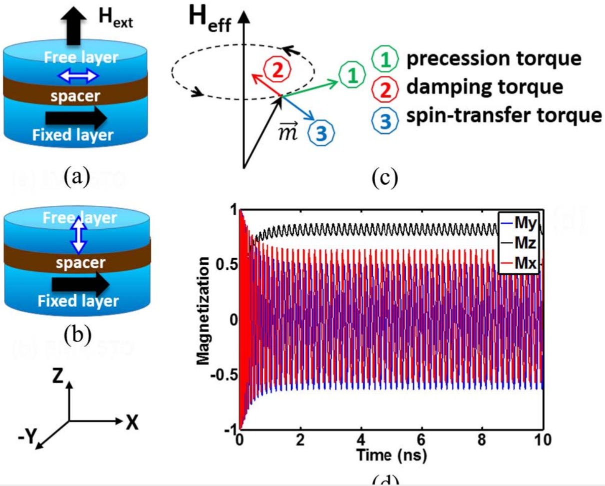
Spin-Torque Oscillator

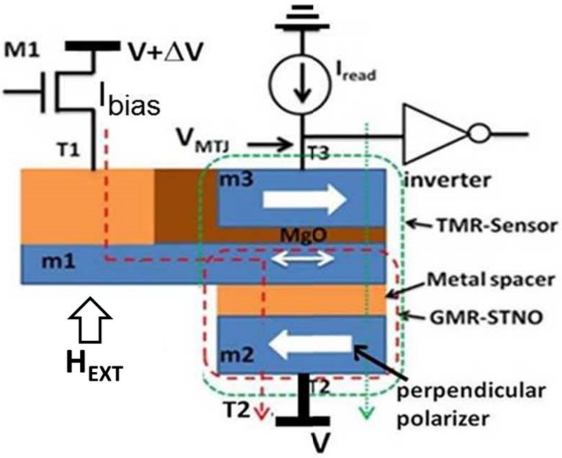


Spin-Torque Oscillator – Two Terminal

Issues

- GMR based STO
  - Can be operated with very low voltage ($\sim$10 mV)
  - The sensed signal amplitude is very low that requires complex sensing circuitry to amplify the signal, leading to high power consumption.
- TMR based STO
  - Requires a large bias voltage, leading to energy inefficiency at the device level
  - Can provide large-amplitude output signals

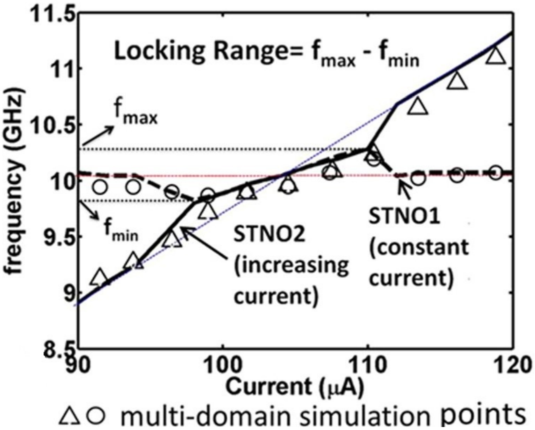
Dual-Pillar STO[M.Sharad,APL,2013]



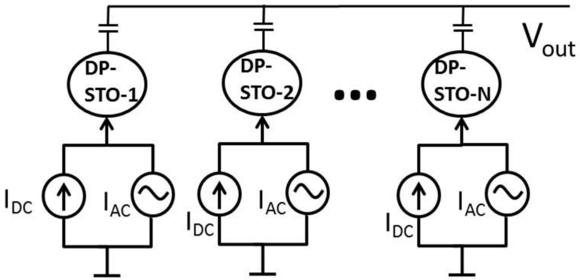
Frequency Locking of Multiple STOs

- Magnetic coupling(Limited by phisical design)
  - Spin wave interaction – Interaction between STOs
  - Dipolar coupling – Facilitate locking of phisically isolated STOs lying in close proximity
- Electrical coupling
- Injection locking

Magnetic coupling

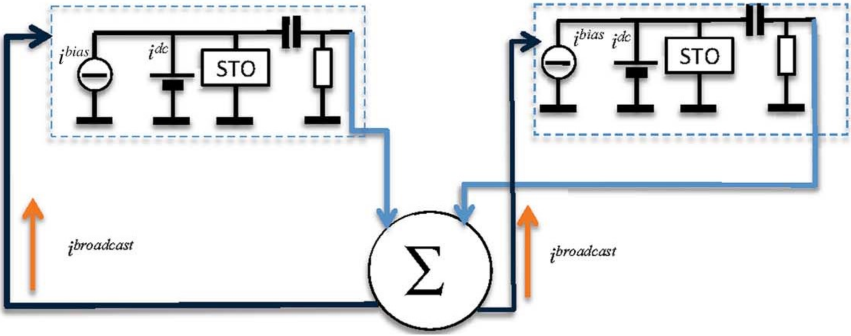


STO Injection Locking[M.Sharad,IEEE.Trans.Magn,2015]



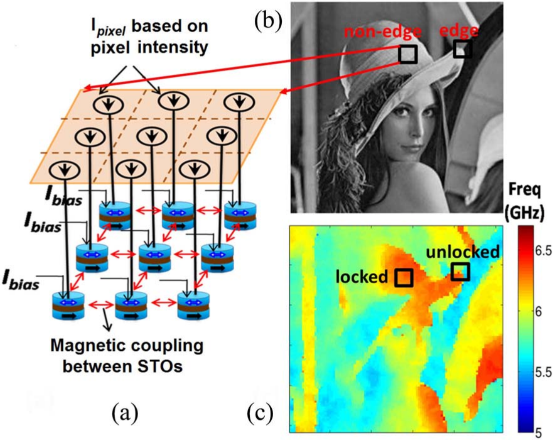
If $f_{I_{AC}} \approx f_{SOT\ biased\ by\ I_{DC}}$, $f_{SOT} = f_{I_{AC}}$.

STO Electrical Coupling[G.Csaba,IEEE.Trans.Magn,2013]



$$i_i^{broadcast} = \frac{1}{M_s N} \sum_{n=1}^{N} C_j M_j^x$$

STO Applications – Image Analysis[M.Sharad,APL,2013]



Process

1) Initialization
2) Pixel → Current → STO
3) Coupling
4) Output

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Reference I

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